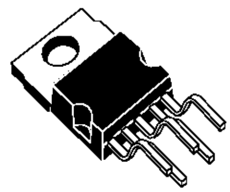
TDA2006

12W AUDIO AMPLIFIER

DESCRIPTION

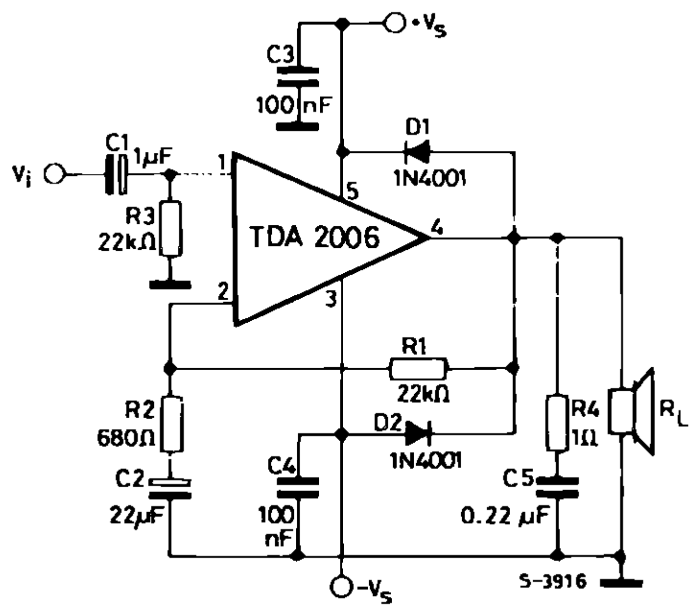
The TDA2006 is a monolithic integrated circuit in Pentawatt package, intended for use as a low frequency class "AB" amplifier. At ±12V, d = 10 % typically it provides 12W output power on a 4Ω load and 8W on a 8Ω . The TDA2006 provides high output current and has very low harmonic and cross-over distortion. Further the device incorporates an original (and patented) short circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the working point of the output transistors within their safe operating area. A conventional thermal shutdown system is also included. The TDA2006 is pin to pin equivalent to the TDA2030.



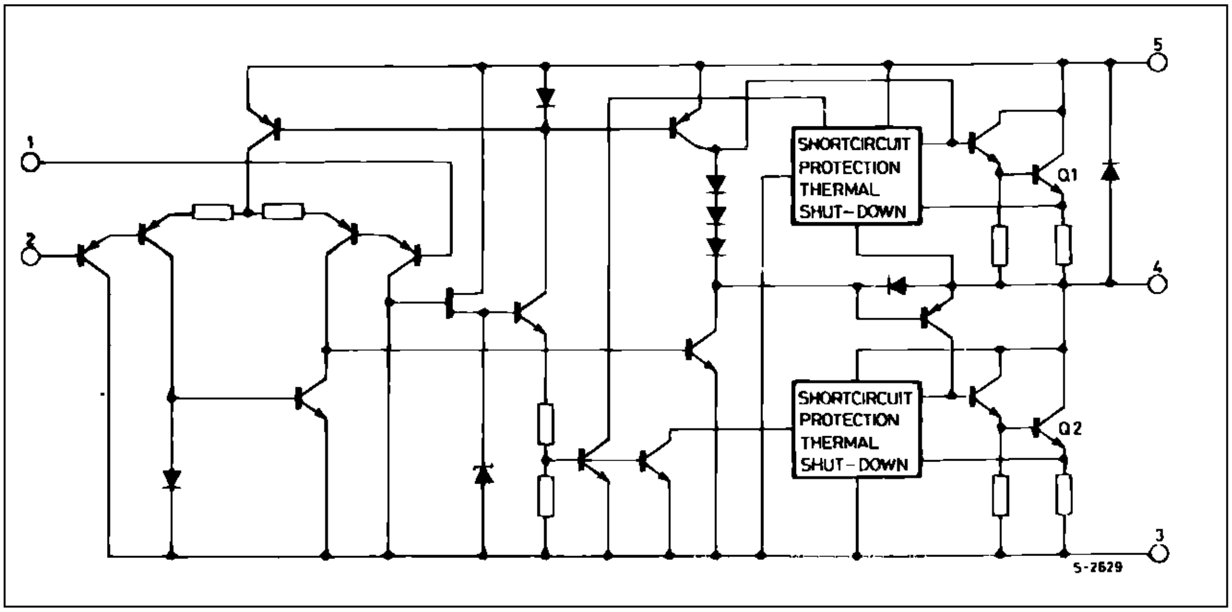
PENTAWATT

ORDERING NUMBERS : TDA2006V
TDA2006H

TYPICAL APPLICATION CIRCUIT



SCHEMATIC DIAGRAM



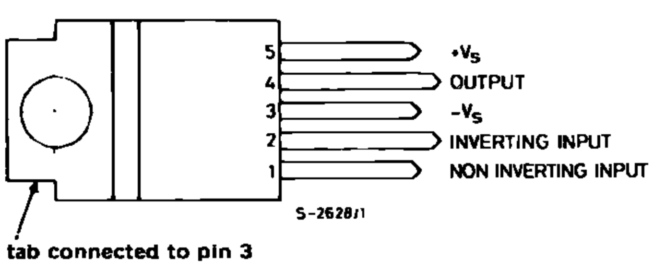
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	± 15	V
V_i	Input Voltage	V_s	
V_i	Differential Input Voltage	± 12	V
I_o	Output Peak Current (internaly limited)	3	A
P_{tot}	Power Dissipation at T_{case} = 90 °C	20	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j-c)}$	Thermal Resistance Junction-case	Max	3	°C/W

PIN CONNECTION



ELECTRICAL CHARACTERISTICS

(refer to the test circuit ; V_S = ± 12V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		± 6		± 15	V
I_d	Quiescent Drain Current	V_s = ± 15V		40	80	mA
I_b	Input Bias Current	V_s = ± 15V		0.2	3	µA
V_{OS}	Input Offset Voltage	V_s = ± 15V		± 8		mV
I_{OS}	Input Offset Current	V_s = ± 15V		± 80		nA
V_{OS}	Output Offset Voltage	V_s = ± 15V		± 10	± 100	mV
P_o	Output Power	d = 10%, f = 1kHz R_L = 4Ω R_L = 8Ω	 6	 12 8		W
d	Distortion	P_o = 0.1 to 8W, R_L = 4Ω, f = 1kHz P_o = 0.1 to 4W, R_L = 8Ω, f = 1kHz		0.2 0.1		% %
V_i	Input Sensitivity	P_o = 10W, R_L = 4Ω, f = 1kHz P_o = 6W, R_L = 8Ω, f = 1kHz		200 220		mV mV
B	Frequency Response (– 3dB)	P_o = 8W, R_L = 4Ω	20Hz to 100kHz			
R_i	Input Resistance (pin 1)	f = 1kHz	0.5	5		MΩ
G_v	Voltage Gain (open loop)	f = 1kHz		75		dB
G_v	Voltage Gain (closed loop)	f = 1kHz	29.5	30	30.5	dB
e_N	Input Noise Voltage	B (– 3dB) = 22Hz to 22kHz, R_L = 4Ω		3	10	µV
i_N	Input Noise Current	B (– 3dB) = 22Hz to 22kHz, R_L = 4Ω		80	200	pA
SVR	Supply Voltage Rejection	R_L = 4Ω, R_g = 22kΩ, f_{ripple} = 100Hz (*)	40	50		dB
I_d	Drain Current	P_o = 12W, R_L = 4Ω P_o = 8W, R_L = 8Ω		850 500		mA mA
T_j	Thermal Shutdown Junction Temperature				145	°C

(*) Referring to Figure 15, single supply.

Figure 1 : Output Power versus Supply Voltage

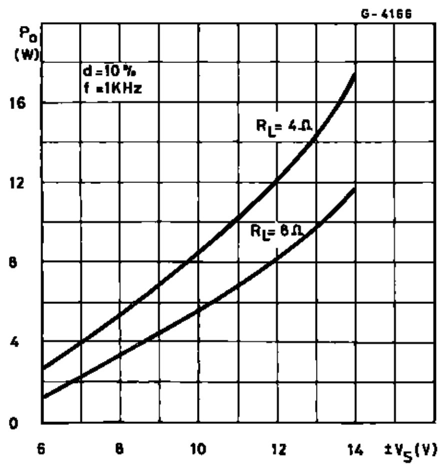


Figure 2 : Distortion versus Output Power

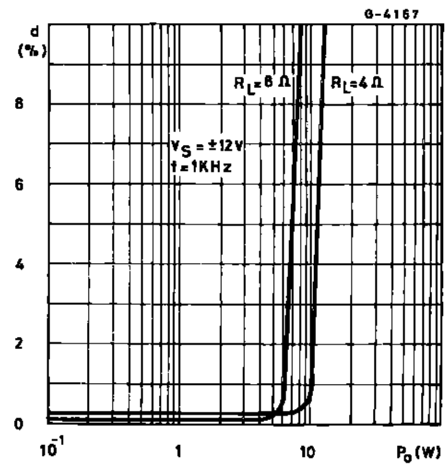


Figure 3 : Distortion versus Frequency

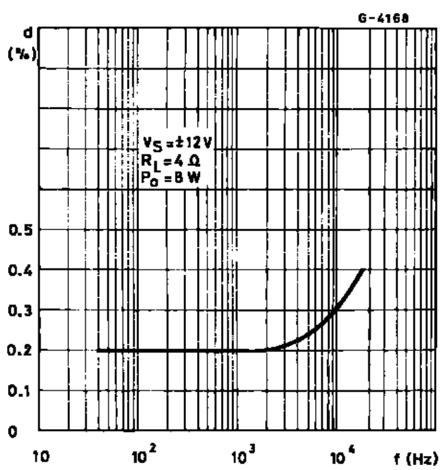


Figure 4 : Distortion versus Frequency

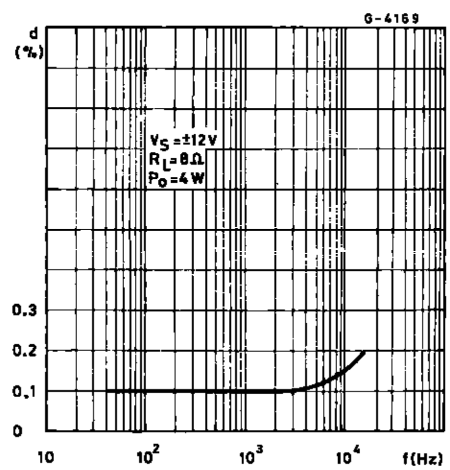


Figure 5 : Sensitivity versus Output Power

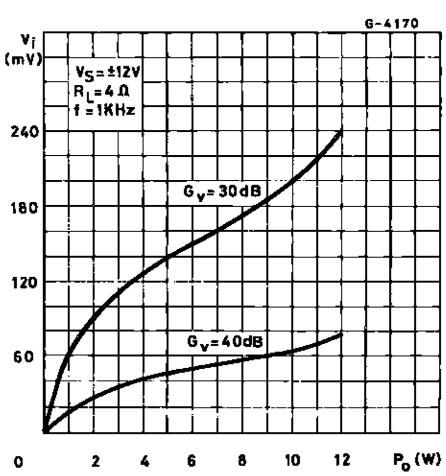


Figure 6 : Sensitivity versus Output Power

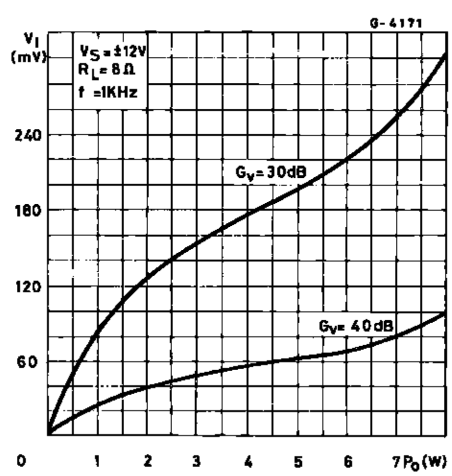


Figure 7 : Frequency Response with different values of the rolloff Capacitor C8 (see Figure 13)

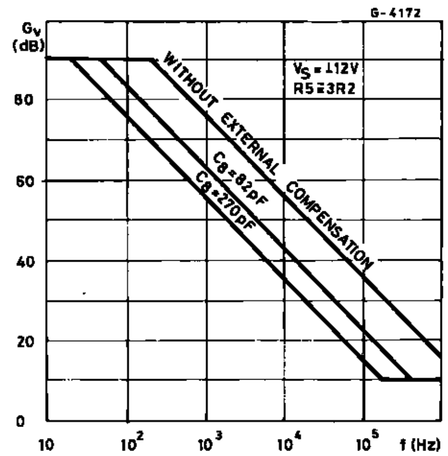


Figure 8 : Value of C8 versus Voltage Gain for different Bandwidths (see Figure 13)

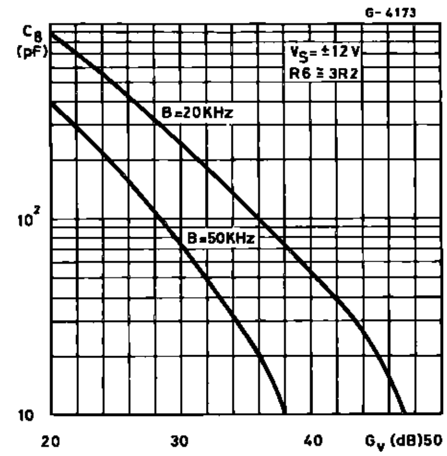


Figure 9 : Quiescent Current versus Supply Voltage

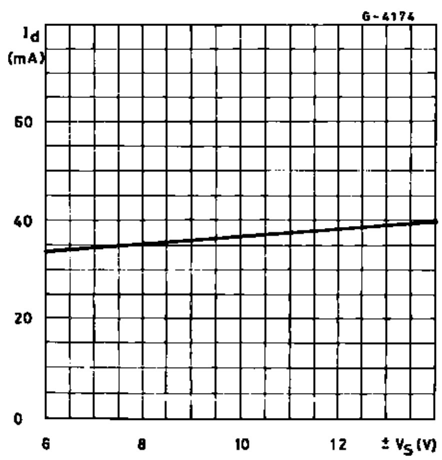


Figure 10 : Supply Voltage Rejection versus Voltage Gain

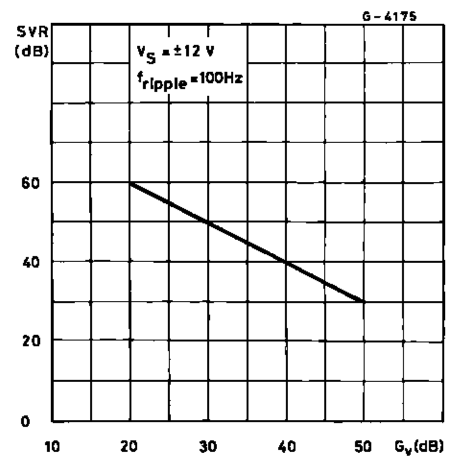


Figure 11 : Power Dissipation and Efficiency versus Output Power

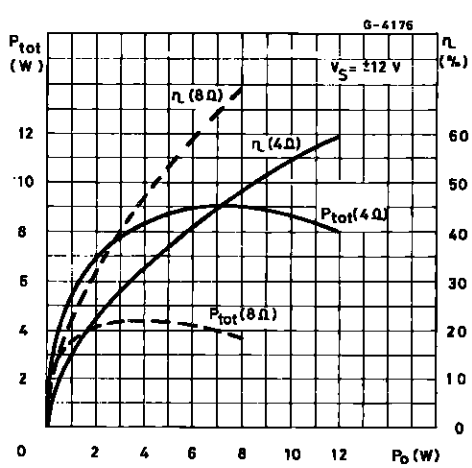


Figure 12 : Maximum Power Dissipation versus Supply Voltage (sine wave operation)

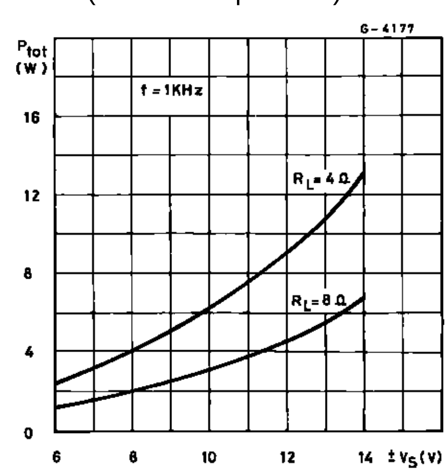


Figure 13 : Application Circuit with Spilt Power Supply

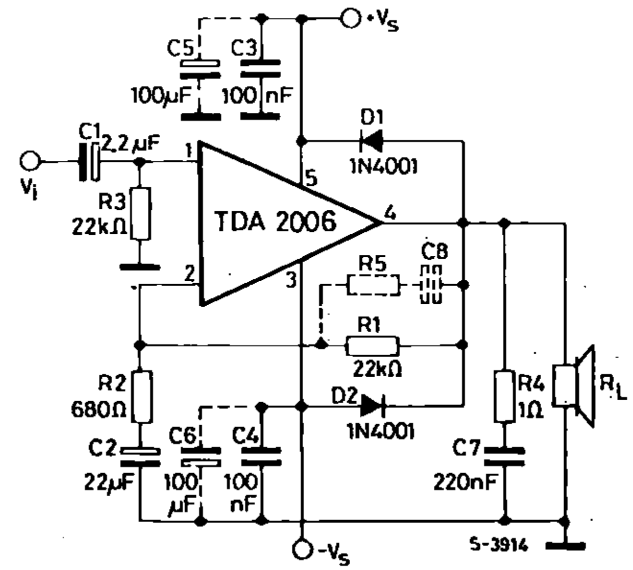


Figure 14 : P.C. Board and Components Layout of the Circuit of Figure 13 (1:1 scale)

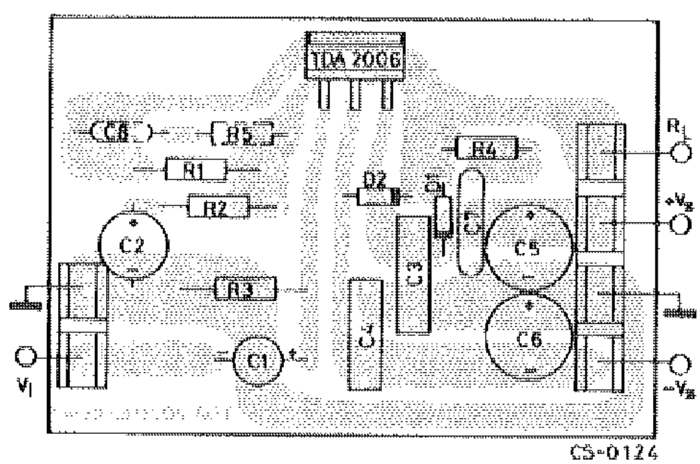


Figure 15 : Application Circuit with Single Power Supply

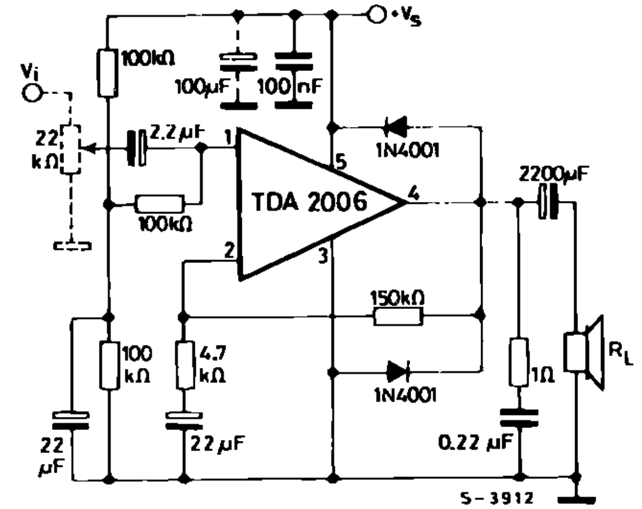


Figure 16 : P.C. Board and Components Layout of the Circuit of Figure 15 (1:1 scale)

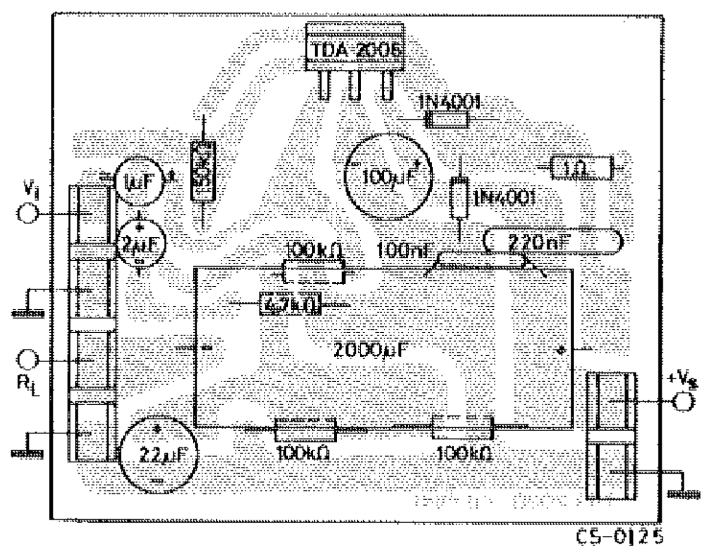
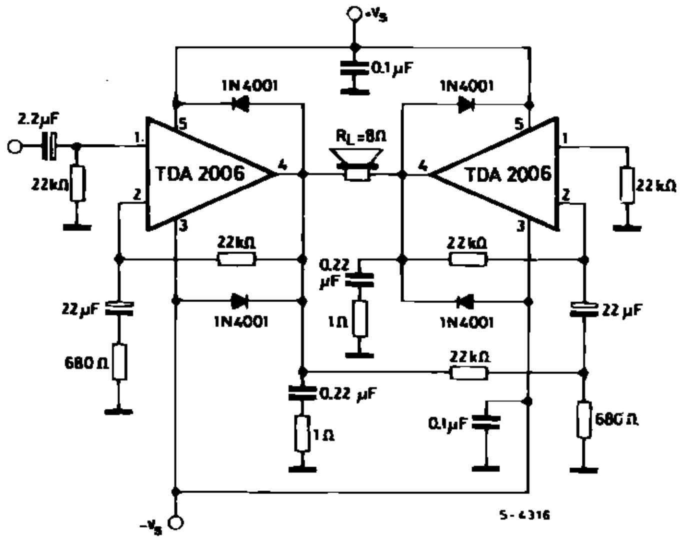


Figure 17 : Bridge Amplifier Configuration with Split Power Supply (P_O = 24W, V_S = ± 12V)



PRACTICAL CONSIDERATIONS

Printed Circuit Board

The layout shown in Figure 14 should be adopted by the designers. If different layout are used, the ground points of input 1 and input 2 must be well decoupled from ground of the output on which a rather high current flows.

Assembly Suggestion

No electrical isolation is needed between the package and the heat-sink with single supply voltage configuration.

Application Suggestion

The recommended values of the components are the ones shown on application circuits of Figure 13. Different values can be used. The table 1 can help the designers.

Table 1

Component	Recommanded Value	Purpose	Larger Than Recommanded Value	Smaller Than Recommanded Value
R_1	22 kΩ	Closed Loop Gain Setting	Increase of Gain	Decrease of Gain (*)
R_2	680 Ω	Closed Loop Gain Setting	Decrease of Gain (*)	Increase of Gain
R_3	22 kΩ	Non Inverting Input Biasing	Increase of Input Impedance	Decrease of Input Impedance
R_4	1 Ω	Frequency Stability	Danger of Oscillation at High Frequencies with Inductive Loads	
R_5	3 R_2	Upper Frequency Cut-off	Poor High Frequencies Attenuation	Danger of Oscillation
C_1	2.2 µF	Input DC Decoupling		Increase of Low Frequencies Cut-off
C_2	22 µF	Inverting Input DC Decoupling		Increase of Low Frequencies Cut-off
C_3C_4	0.1 µF	Supply Voltage by Pass		Danger of Oscillation
C_5C_6	100 µF	Supply Voltage by Pass		Danger of Oscillation
C_7	0.22 µF	Frequency Stability		Danger of Oscillation
C_8	$\frac{1}{2\pi BR_1}$	Upper Frequency Cut-off	Lower Bandwidth	Larger Bandwidth
D_1D_2	1N4001	To Protect the Device Against Output Voltage Spikes.		

(*) Closed loop gain must be higher than 24dB.

SHORT CIRCUIT PROTECTION

The TDA2006 has an original circuit which limits the current of the output transistors. Figure 18 shows that the maximum output current is a function of the collector emitter voltage ; hence the output transistors work within their safe operating area (Figure 19).

This function can therefore be considered as being peak power limiting rather than simple current limiting.

It reduces the possibility that the device gets damaged during an accidental short circuit from AC output to ground.

THERMAL SHUT DOWN

The presence of a thermal limiting circuit offers the following advantages :

1) an overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since the T_j cannot be higher than 150°C.
2) the heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature.

If for any reason, the junction temperature increases up to 150 °C, the thermal shutdown simply reduces the power dissipation and the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance) ; Figure 22 shows the dissipable power as a function of ambient temperature for different thermal resistances.

Figure 18 : Maximum Output Current versus Voltage $V_{CE\ (sat)}$ accross each Output Transistor

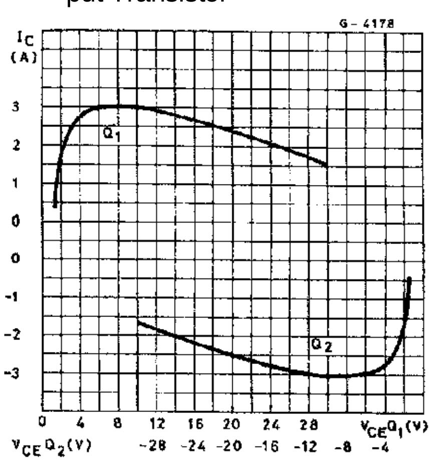


Figure 19 : Safe Operating Area and Collector Characteristics of the Protected Power Transistor

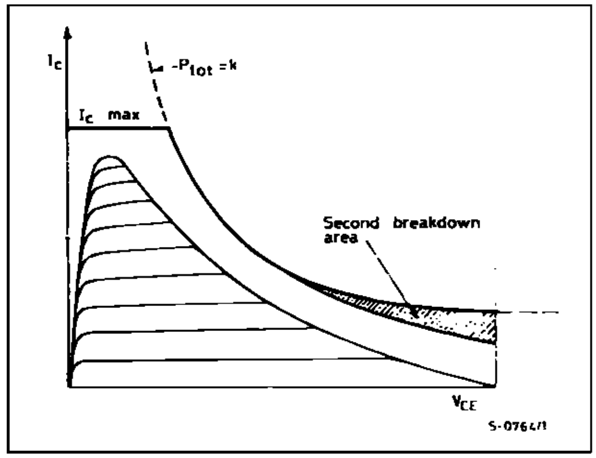


Figure 20 : Output Power and Drain Current versus Case Temlperature (R_L = 4Ω)

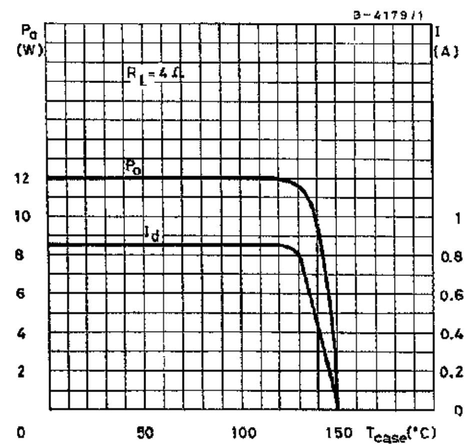


Figure 21 : Output Power and Drain Current versus Case Temlperature (R_L = 8Ω)

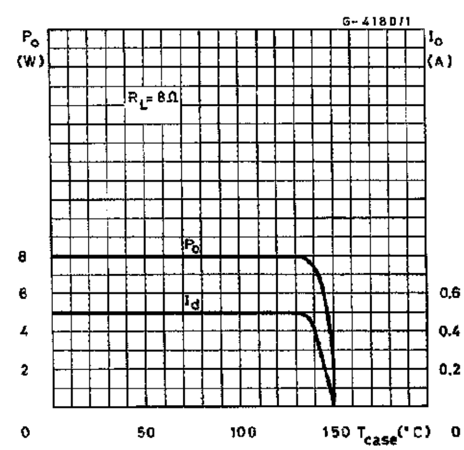
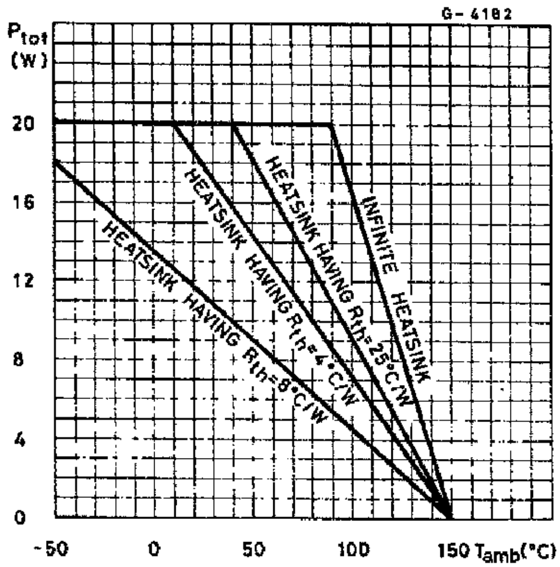


Figure 22 : Maximum Allowable Power Dissipation versus Ambient Temperature

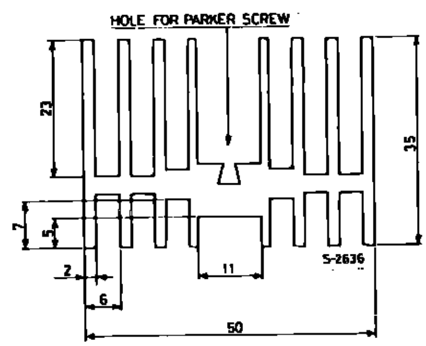


DIMENSION SUGGESTION

The following table shows the length of the heatsink in Figure 23 for several values of P_{tot} and R_{th}.

P_{tot} (W)	12	8	6
Lenght of Heatsink (mm)	60	40	30
R_{th} of Heatsink (°C/W)	4.2	6.2	8.3

Figure 23 : Example of Heatsink



PENTAWATT PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			4.8			0.189
C			1.37			0.054
D	2.4		2.8	0.094		0.110
D1	1.2		1.35	0.047		0.053
E	0.35		0.55	0.014		0.022
F	0.8		1.05	0.031		0.041
F1	1		1.4	0.039		0.055
G		3.4		0.126	0.134	0.142
G1		6.8		0.260	0.268	0.276
H2			10.4			0.409
H3	10.05		10.4	0.396		0.409
L		17.85			0.703	
L1		15.75			0.620	
L2		21.4			0.843	
L3		22.5			0.886	
L5	2.6		3	0.102		0.118
L6	15.1		15.8	0.594		0.622
L7	6		6.6	0.236		0.260
M		4.5			0.177	
M1		4			0.157	
Dia	3.65		3.85	0.144		0.152

